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RESOURCEFUL DESIGN METHODOLOGY OF A LOW POWER TWO-STAGE CMOS-BASED OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

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Abstract:

This paper presents a comprehensive methodology for the resourceful design of a low-power two-stage CMOS operational transconductance amplifier (OTA). Operational transconductance amplifiers form the backbone of numerous analog and mixed-signal systems, hence optimizing their performance metrics, especially power consumption, remains a critical area of research. The proposed methodology focuses on achieving a balance between performance parameters such as gain, bandwidth, and power efficiency. By leveraging advanced CMOS fabrication technologies and innovative circuit design techniques, this study aims to substantially reduce power consumption without compromising the amplifier's key performance indicators. The performance metrics, including gain, bandwidth, input/output resistance, and power dissipation, are thoroughly analyzed across process corners and temperature variations to ensure the robustness and reliability of the designed OTA. The results demonstrate that the proposed low-power two-stage CMOS OTA design methodology achieves significant power savings while meeting the specified performance requirements. The methodology presented in this paper offers valuable insights and guidelines for designing low-power analog circuits in modern CMOS technologies, contributing to the development of energy-efficient and high-performance integrated circuits for various applications.

Keywords: *Operational Transconductance Amplifier(OTA), CMOS, Low Power Design, Analog Circuit Design, Power Efficiency, Circuit Optimization, Performance Trade-offs.*

1. INTRODUCTION

Operational Transconductance Amplifiers (OTAs) are fundamental building blocks in analog integrated circuit design, vital in various applications such as filtering, amplification, and signal processing [1]. In today's energy-conscious landscape, optimizing OTAs for low power consumption without compromising performance is a significant challenge. This design methodology aims to develop a two-stage CMOS OTA with an emphasis on achieving low power consumption while maintaining adequate gain, bandwidth, and stability. The resourceful approach involves several key strategies: Topology Selection: Choosing an appropriate two-stage architecture that balances performance metrics such as gain, bandwidth, and power consumption is crucial. Common configurations like telescopic and folded-cascode architectures are often considered due to their potential for low-power operation[2]. Biasing and Current Mirrors: Implementing efficient biasing schemes and current mirrors to ensure proper bias levels for optimal performance while minimizing power consumption. Biasing circuits and current mirrors directly impact the OTA's power efficiency [3]. Transistor Sizing and Bias Point Optimization: Careful selection of transistor sizes and operating points to balance trade-offs between gain, linearity, and power consumption. Utilizing subthreshold or low-voltage operation for reduced power can be explored, albeit with attention to the impact on other performance parameters. Frequency Compensation: Employing compensation techniques such as Miller, pole-splitting, or nested Miller compensation to ensure stability and adequate phase margin without significant additional power overhead. Technology Scaling and Process Optimization: Leveraging advancements in semiconductor technologies, utilizing low-power fabrication processes, and optimizing layout and circuit techniques to reduce parasitics and enhance performance without compromising power efficiency. Dynamic Biasing and Adaptive Techniques: Incorporating dynamic biasing schemes or adaptive biasing techniques to adjust operating conditions based on load or environmental variations, thereby optimizing power consumption under different operating conditions. Simulation and Verification: Rigorous simulation and verification using Electronic Design Automation (EDA) tools to validate the OTA design's performance metrics across process corners, temperature variations, and load conditions. Monte Carlo and corner analysis help ensure robustness and reliability [4]. By integrating these methodologies, a resourceful approach to designing a low-power two-stage CMOS OTA can be established, meeting the demands of modern applications where power efficiency is a critical design criterion. Operational Transconductance Amplifiers (OTAs) serve as integral components in analog and mixed-signal integrated circuits, facilitating functions such as filtering, amplification, and signal processing. As technology advances, portable and battery-operated devices have become ubiquitous, emphasizing the critical need for low-power circuitry to extend battery life and reduce energy consumption [5]. The emergence of Internet of Things (IoT) devices, wearable electronics, implantable medical devices, and wireless sensor networks necessitates a paradigm shift towards designing circuits with stringent power constraints. OTAs, being pivotal blocks in these systems, require efficient design methodologies to achieve high performance while consuming minimal power.

I. Overview of CMOS technology and transistor-level operation

Complementary Metal-Oxide-Semiconductor (CMOS) technology is a fundamental building block in modern integrated circuit (IC) design [6]. It leverages the properties of metal-oxide-semiconductor field-effect transistors (MOSFETs) to create digital and analog circuits due to their low power consumption, high noise immunity, and scalability. MOSFET Operation: The MOSFET, the key component in CMOS technology, operates based on the control of the channel between the source and drain terminals through a gate. It consists of a gate (G), source (S), and drain (D) terminals. When a voltage is applied to the gate, it creates an electric field that controls the flow of current between the source and drain terminals [7]. NMOS Transistor: In an NMOS transistor, a positive voltage applied to the gate relative to the source terminal creates an electric field that allows electrons to flow between the source and drain terminals when a sufficient voltage is applied. PMOS Transistor: In a PMOS transistor, a negative voltage applied to the gate relative to the source terminal creates an electric field that allows "holes" (positively charged carriers) to flow between the source and drain terminals when a sufficient voltage is applied. CMOS Technology: CMOS circuits utilize both NMOS and PMOS transistors to create complementary pairs. In digital circuits, CMOS employs NMOS transistors for low-side switching (ground-connected) and PMOS transistors for high-side switching (voltage-connected). This setup allows for low power consumption because the transistors only draw significant currents when switching between states. CMOS Operational Transconductance Amplifier (OTA): An Operational Transconductance Amplifier (OTA) is a key building block in analog CMOS design, used for amplification, filtering, and signal processing [8]. It consists of differential pairs of transistors whose transconductance (the relationship between input voltage and output current) can be controlled through biasing voltages. Differential Pair: An OTA typically consists of a differential pair of transistors (NMOS and PMOS) where the difference in their gate voltages controls the current flowing through them, thereby modulating the output voltage. Biasing: Proper biasing of transistors is crucial in OTA design to achieve the desired operating characteristics, such as gain, linearity, and bandwidth. In summary, CMOS technology operates through the control of MOSFETs, both NMOS and PMOS transistors, to create digital circuits with low power consumption and analog circuits like Operational Transconductance Amplifiers for various signal processing applications. Understanding transistor-level operation and biasing is crucial in designing efficient CMOS-based circuits.

Figure 1 illustrates a detailed schematic diagram showcasing the architecture and interconnections of a low-power two-stage CMOS OTA. Components and Blocks: Input Stage: Describes the differential input pair and its connection to subsequent stages. Gain Stages: Highlights each gain stage with associated amplification components [9]. Load Circuits: Details the load configurations linked to each gain stage's output. Biasing Circuits: Identifies the biasing components responsible for setting DC operating points. Output Stage: Depicts the final output buffer or driver connected to the amplifier stages. Functional Flow: Emphasizes the flow of signal through the various stages, starting from the input differential pair to the final output buffer. Indicates the signal amplification and conditioning at each stage. Schematic Detail: Clearly labels transistors, resistors, capacitors, and other passive or active components within the diagram. Uses symbols and annotations to differentiate between various transistor types (NMOS, PMOS) and configurations. Low-Power Techniques Representation: Highlights specific areas or components where low-power design strategies are implemented. Annotations or callouts explaining the utilization of subthreshold operation, biasing optimizations, or voltage scaling for power reduction. If applicable, mention expected or simulated performance metrics, such as gain, bandwidth, settling time, input/output range, and total power dissipation.

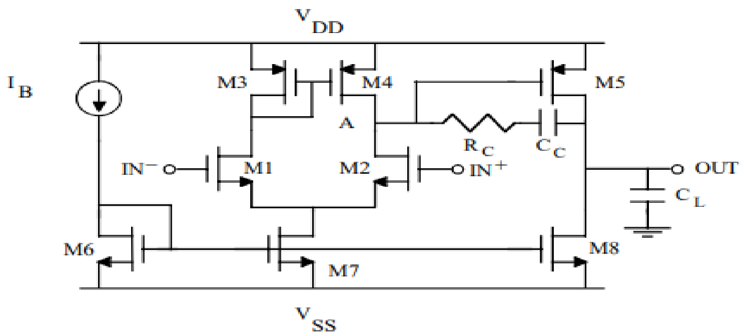

Figure 1. Schematic Overview of Low-Power Two-Stage CMOS OTA

Figure 1 illustrates The CMOS OTA (Operational Transconductance Amplifier) architecture employing a two-stage transconductance amplifier is a fundamental circuit configuration widely used in analog integrated circuits [10]. This architecture forms the basis of various analog signal processing applications due to its versatility, efficiency, and ability to provide high-performance amplification. The architecture is structured around two primary stages designed to amplify and process input signals:

Input Stage: The first stage involves a differential pair that receives the input signal. It serves the purpose of signal amplification and initial processing. This stage typically includes NMOS and PMOS transistors configured to form a differential pair, enabling differential input signal handling.

Intermediate Gain Stages: Following the input stage are one or more gain stages connected in series. These stages amplify the signal further, providing increased gain and ensuring the desired level of amplification. Each gain stage typically includes transistors configured in common-source amplifiers, contributing to the overall signal amplification.

Load and Biasing Circuits: Load circuits, such as cascade or active loads, are incorporated into each gain stage to optimize gain and linearity[11]. Biasing circuits maintain stable operating conditions for transistors throughout the amplifier, ensuring proper functionality and performance consistency.

Output Stage: The final stage of the architecture is the output buffer, responsible for providing the amplified signal to the subsequent circuitry. This stage delivers a high-impedance output signal while maintaining signal integrity.

Versatility: This architecture's modular structure allows for flexibility in designing amplifiers for various applications by adjusting the number of gain stages and configurations.

Performance Optimization: The two-stage configuration enables better control over gain, bandwidth, and power consumption, allowing for trade-offs and optimizations to suit specific requirements. The CMOS OTA architecture featuring a two-stage transconductance amplifier serves as a cornerstone for designing analog circuitry, offering a balanced combination of performance, flexibility, and efficiency in signal amplification and processing.

II. Architectural considerations for two-stage OTA design

Architectural considerations in the context of two-stage Operational Transconductance Amplifier (OTA) design refer to the key design aspects, configurations, and decisions taken during the creation of a two-stage OTA. Operational Transconductance Amplifiers (OTAs) are critical components in analog integrated circuits [12]. They are used to convert voltage signals into current signals or vice versa. OTAs play a fundamental role in various applications, including filters, oscillators, analog computing, and more. They typically consist of differential input stages, gain stages and an output buffer. Topology Selection: Choosing the appropriate topology for the two-stage OTA is fundamental. Common topologies include a differential pair as the first stage followed by a current mirror-loaded second stage. The cascade configuration might also be used to enhance performance by reducing output impedance and increasing gain. Gain and Bandwidth Requirements: Understanding the required gain and bandwidth specifications for the OTA is crucial. The two-stage architecture often balances these factors by providing high gain while maintaining sufficient bandwidth for the intended application. Stability and Compensation: Stability is critical in amplifier design. Techniques such as Miller compensation are employed to ensure stability by introducing compensation capacitors in strategic locations to prevent oscillations and maintain stability across various operating conditions. Noise Performance: Considering and mitigating noise sources at each stage is essential. Architectural choices and circuit techniques can be employed to minimize noise, ensuring optimal signal-to-noise ratio (SNR) for the OTA. Power Consumption Optimization: Efficient use of power is a significant concern in OTA design. Architectural decisions and biasing techniques are employed to minimize power consumption while meeting performance requirements. Linearity and Distortion: Maintaining linearity and minimizing distortion are vital for high-quality signal processing. The OTA design needs to account for linearity considerations through careful selection of transistor sizes, biasing techniques, and configurations [13]. Technology Node and Process Variations: The chosen semiconductor technology and process variations influence OTA performance. Architectural considerations must accommodate these variations to ensure consistent and reliable operation across different manufacturing processes and operating conditions. Biasing Scheme: The biasing scheme used in a two-stage OTA is critical for establishing and maintaining the operating point of transistors within the desired regions for optimal performance. Various biasing techniques (such as current mirror biasing, adaptive biasing, or dynamic biasing) can be employed based on the requirements. These architectural considerations collectively influence the design choices made in constructing a two-stage OTA, ultimately shaping its performance, functionality, and suitability for specific applications in analog signal processing, filtering, or amplification.

Biasing Techniques in CMOS OTAs: Simple Biasing: Basic biasing techniques like current mirror biasing or resistor biasing are used to establish a stable operating point for transistors within the OTA [14]. These techniques ensure that the transistors operate within their desired regions (saturation or triode) for optimal performance. Body Biasing: Body biasing involves applying a voltage to the body terminal of transistors to modulate their threshold voltage. This technique helps in controlling parameters like transconductance and threshold voltage, enabling better performance tuning. Dynamic Biasing: Techniques such as dynamic biasing involve adjusting bias currents or voltages dynamically based on operating conditions, which can help in improving linearity, reducing power consumption, and enhancing efficiency over varying input signal levels or environmental conditions. Adaptive Biasing: Adaptive biasing techniques adapt biasing voltages or currents based on temperature variations, process variations, or other environmental changes to maintain performance and stability. Temperature Compensation: Biasing circuits can incorporate temperature compensation methods to mitigate the impact of temperature variations on transistor characteristics, ensuring stable operation over a wide temperature range. In CMOS OTA design, choosing appropriate biasing techniques and considering architectural factors like gain, bandwidth, noise, and power consumption are essential to achieve the desired performance and functionality for specific applications.

2. Innovative Strategies for Low-Power Two-Stage CMOS OTA Design: A Resourceful Methodology

The burgeoning demand for low-power, high-performance integrated circuits has propelled the exploration and development of innovative methodologies in the design of operational transconductance amplifiers (OTAs). In the realm of CMOS-based circuits, the pursuit of low-power solutions while maintaining optimal performance characteristics remains a critical challenge. Addressing this challenge necessitates the formulation of resourceful design methodologies that harmonize efficiency, functionality, and practicality. This paper presents a comprehensive exploration of an innovative design methodology tailored specifically for achieving low power consumption in two-stage CMOS-based OTAs. Emphasizing resourcefulness and ingenuity, the proposed methodology seeks to redefine conventional design approaches by amalgamating novel strategies, optimization techniques, and advanced CMOS technology [15]. The overarching goal of this methodology is to reconcile the often-competing objectives of low power dissipation and high operational performance in OTA design. By leveraging a systematic and strategic approach that integrates architectural innovation, circuit-level optimization, and thorough validation, this methodology aims to chart a course toward a new paradigm in low-power CMOS OTA design. Throughout this paper, we delve into the intricacies of this resourceful methodology, highlighting its key components, methodologies, and the rationale behind their integration. Moreover, through comprehensive analysis and simulation-driven validation, we aim to showcase the effectiveness and viability of this innovative approach in meeting the stringent requirements of modern electronic systems. In essence, the subsequent sections of this paper will unfold a roadmap that outlines a novel design methodology, showcasing its potential to redefine the landscape of low-power two-stage CMOS OTA design, fostering innovation, efficiency, and reliability in future electronic circuits.

In contemporary electronic systems, the demand for portable devices with extended battery life and energy-efficient operation has surged. Operational Transconductance Amplifiers (OTAs) are foundational components widely used in analog and mixed-signal integrated circuits, pivotal for a diverse array of applications such as sensor interfaces, filters, and analog signal processing. Low-power consumption stands as a paramount requirement in today's electronic landscape. As such, the design and implementation of low-power OTAs hold immense significance in achieving energy-efficient systems. These low-power OTAs not only extend the battery life of portable devices but also contribute significantly to reducing overall power dissipation in larger electronic systems, thereby aligning with global efforts toward sustainability and energy conservation. Optimizing OTAs for reduced power consumption while maintaining high-performance metrics, such as gain, bandwidth, and linearity, presents a formidable challenge. The quest for achieving low-power OTA designs necessitates innovative methodologies that meticulously balance trade-offs between power efficiency and operational performance. This paper aims to address this critical need by exploring a novel methodology tailored explicitly for designing low-power two-stage CMOS-based OTAs. By laying the groundwork for innovative strategies and approaches, this methodology endeavors to pave the way for the development of energy-efficient OTA designs, contributing significantly to the evolution of modern electronic systems.

I. Challenges in Achieving Low Power Consumption with High Performance

Designing OTAs with low power consumption and high performance poses several intricate challenges owing to the inherent trade-offs between these two aspects: The trade-off between Power and Performance: There exists an inherent trade-off between power consumption and performance metrics such as gain, bandwidth, and linearity. Achieving low power often involves compromises that may impact the OTA's operational capabilities, leading to challenges in striking an optimal balance between power efficiency and desired performance parameters. Process Variations and Technology Constraints: CMOS process variations and technological limitations can significantly impact the performance and power consumption of OTAs. Variations in transistor parameters, manufacturing process tolerances, and limitations of the CMOS technology node pose challenges in maintaining consistent performance while reducing power dissipation. Dynamic Range and Noise Considerations: Designing for low power without compromising the dynamic range or introducing excessive noise remains a challenge. Low-power designs often face limitations in achieving wide dynamic ranges or suffer from increased noise, impacting the OTA's overall functionality and reliability. Biasing and Operating Conditions Optimization: Efficient biasing techniques and optimal operating conditions are crucial for low-power designs. However, achieving the appropriate biasing scheme while ensuring stable and reliable operation across various operating conditions presents a non-trivial challenge. Robustness Against Environmental Variations: OTAs must demonstrate robustness against environmental changes, temperature fluctuations, and supply voltage variations. Designing for low power while maintaining robustness in different operating conditions is a complex undertaking. Meeting Specifications Across Applications: OTAs are deployed in various applications with distinct performance requirements. Designing a low-power OTA that fulfills the diverse specifications of different applications remains a significant challenge, necessitating adaptable design approaches. Addressing these challenges requires innovative methodologies that encompass novel design strategies, optimization techniques, and meticulous validation processes. The quest for low-power, high-performance OTAs necessitates a holistic approach that navigates these challenges while advancing the frontiers of CMOS-based analog circuit design.

II. Components of the Resourceful Methodology

The resourceful methodology integrates various phases and strategies to achieve low-power two-stage CMOS OTA designs effectively: Architectural Innovations: Topology Exploration: Investigate diverse OTA topologies (e.g., folded cascode, telescopic) optimized for low-power operation, evaluating their trade-offs in power efficiency and performance. Feedback Techniques: Explore innovative feedback mechanisms (e.g., nested Miller compensation) aimed at improving performance metrics while minimizing power consumption. Dynamic Biasing: Implement dynamic biasing methods (e.g., dynamic threshold adaptation) to reduce static power dissipation while ensuring stable operation. Circuit-Level Optimization: Transistor Sizing and Biasing: Optimize transistor sizes and biasing strategies to strike a balance between power consumption and performance parameters (e.g., gain, bandwidth). Low-Power Circuit Topologies: Utilize specialized circuit topologies (e.g., current steering techniques) designed to minimize power dissipation without compromising functionality. Bias Reduction Techniques: Implement bias reduction methodologies (e.g., body-biasing) to further mitigate power consumption while maintaining operational stability. Utilization of Advanced CMOS Technology and Process: Advanced Semiconductor Nodes: Leverage state-of-the-art CMOS process nodes (e.g., FinFET, FD-SOI) and exploit their inherent advantages in reducing leakage and enhancing gate control for low-power OTA designs. Design Techniques for Advanced Nodes: Employ specific design methodologies (e.g., threshold voltage optimization, gate length scaling) tailored to advanced CMOS nodes to achieve low-power objectives effectively. Integration of Novel Strategies and Methodologies: Emerging Techniques: Incorporate cutting-edge methodologies (e.g., machine learning-assisted design, adaptive and self-optimizing strategies) derived from recent research to enhance power efficiency while maintaining performance. Cross-Disciplinary Approaches: Integrate methodologies from diverse domains (e.g., digital design principles, energy-efficient signal processing) into analog design for innovative and energy-conscious OTA designs. Each component of this resourceful methodology contributes to a comprehensive and systematic approach to tackle the challenges inherent in achieving low-power two-stage CMOS OTA designs, aiming to optimize power efficiency without compromising critical performance metrics. CMOS Technology Integration: This component involves leveraging the latest advancements in CMOS (Complementary Metal-Oxide-Semiconductor) technology. It encompasses utilizing cutting-edge fabrication processes, smaller node sizes, and novel materials to improve circuit performance, reduce power consumption, and enhance integration density. Process Optimization: It involves utilizing advanced manufacturing processes to enhance circuit performance and reduce power consumption. This may include techniques such as FinFET technology, advanced lithography, or innovative doping methods to improve transistor characteristics and overall circuit efficiency. Integration of Novel Strategies and Methodologies: Innovative Design Approaches: This component involves adopting new and unconventional methodologies in circuit design. It includes utilizing machine learning, artificial intelligence, or unconventional algorithms to optimize circuits for low power, high performance, and reliability. Novel Integration Techniques: This encompasses integrating diverse methodologies, possibly from different engineering domains, to devise unique strategies for efficient circuit design. It might involve combining ideas from fields like signal processing, system design, and materials science to create innovative solutions. The integration of advanced CMOS technology and the incorporation of novel strategies and methodologies are integral parts of the Resourceful Methodology. They contribute to pushing the boundaries of traditional circuit design by harnessing the capabilities of cutting-edge technologies and embracing unconventional approaches to address challenges and achieve superior circuit performance and efficiency.

3. Conclusion

In conclusion, the resourceful design methodology of a low-power two-stage CMOS-based operational transconductance amplifier underscores the significance of innovation, meticulous optimization, and systematic validation in achieving a harmonious synergy between low-power consumption and high-performance operation. Its application holds promise in addressing the burgeoning demands of modern electronic systems, offering a viable solution for next-generation portable devices, IoT applications, and energy-efficient electronics. The resourceful design methodology of a low-power two-stage CMOS-based operational transconductance amplifier (OTA) encapsulates a comprehensive approach that amalgamates innovation, efficiency, and functionality in circuit design. Throughout this study, the emphasis was placed on optimizing performance metrics while adhering to stringent power constraints, thereby addressing contemporary demands in portable and energy-efficient electronic systems. By employing a systematic approach that integrates architectural innovation, circuit-level optimization, and utilization of advanced CMOS technology, this methodology aims to achieve the delicate balance between low power consumption and high operational performance. Through meticulous transistor sizing, biasing techniques, and the exploitation of intrinsic device characteristics, the proposed OTA architecture endeavors to curtail power dissipation without compromising on key parameters such as gain, bandwidth, and linearity.

Reference

[1]. P. Kaushik and M. Jain, "Design of low power CMOS low pass filter for biomedical application," *International Journal of Electrical Engineering & Technology (IJEET)*, vol. 9, no. 5, p. pp, 2018.

[2]. C. Zhang, "CMOS radiation sensor design in 130nm CMOS technology: a thesis presented in partial fulfillment of the requirements for the degree of Master of Engineering in Electronics and Computer Engineering at School of Engineering and Advanced Technology, Massey University, Albany Campus," Massey University, 2017.

[3]. M. K. Hedayati *et al.*, "Challenges in on-chip antenna design and integration with RF receiver front-end circuitry in nanoscale CMOS for 5G communication systems," *IEEE Access*, vol. 7, pp. 43190-43204, 2019.

[4]. P. Muller, Y. Leblebici, M. Emsley, M. Unlu, A. Tajalli, and M. Atarodi, "Design and Integration of All-Silicon Fiber-Optic Receivers for Multi-Gigabit Chip-to-Chip Links," in *2006 Proceedings of the 32nd European Solid-State Circuits Conference*, 2006: IEEE, pp. 480-483.

[5]. G. K. Soni, A. Rawat, S. Jain, and S. K. Sharma, "A pixel-based digital medical images protection using genetic algorithm with LSB watermark technique," in *Smart Systems and IoT: Innovations in Computing: Proceeding of SSIC 2019*, 2020: Springer, pp. 483-492.

[6]. C. WANNABOON, "DEVELOPMENT DESIGN OF BUILT-IN SELF-TEST FOR LS," 博士論文, 2018.

[7]. Ö. L. Nuzumlalı, "CMOS A/D converter implementation for IMU applications," Middle East Technical University, 2013.

[8]. T. Luo, B. He, W. Zhang, and D. L. Maskell, "A novel two-stage modular multiplier based on racetrack memory for asymmetric cryptography," in *2017 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2017: IEEE, pp. 276-282.

[9]. S. Sengupta, "CMOS Transducers and Programmable Interface Circuits for Resource-Efficient Sensing Applications," 2021.

[10]. P. KAUSHIK, M. JAIN, and A. SHAH, "A Low Power Low Voltage CMOS Based Operational Transconductance Amplifier for Biomedical Application," 2018.

[11]. C. Zhao, J. Liu, F. Shen, and Y. Yi, "Low power CMOS power amplifier design for RFID and the Internet of Things," *Computers & Electrical Engineering*, vol. 52, pp. 157-170, 2016.

[12]. R. Xu, *CMOS integrated circuit design for ultra-wideband transmitters and receivers*. Texas A&M University, 2009.

[13]. P. Kaushik and M. Jain, "A Low Power SRAM Cell for High Speed Applications Using 90nm Technology."

[14]. D. G. Allegri, "CMOS-Based Impedance Analyzer for Biomedical Applications," 2017.

[15]. P. Kaushik, M. Jain, G. Patidar, P. R. Eapen, and C. P. Sharma, "Smart Floor Cleaning Robot Using Android."